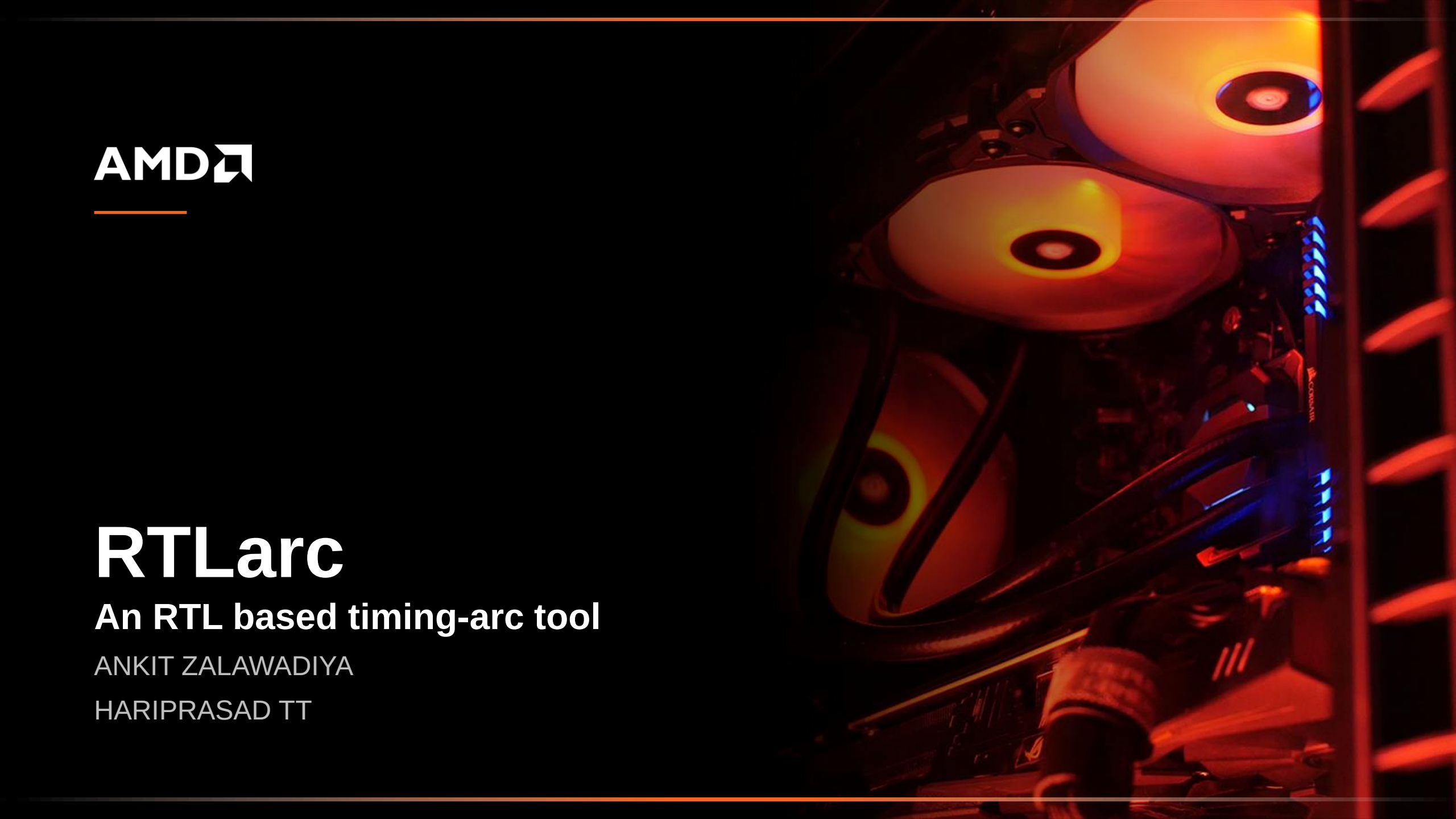


RTLarc

An RTL based timing-arc tool

ANKIT ZALAWADIYA

HARIPRASAD TT

MOTIVATION

- Timing model generation is one of the most important aspects of IP design.
- Timing Characterization
  - Means capturing timing-arcs in .lib/.db.
  - Important to model at IP level as affects SoC level timing closure.
- Missing timing-arcs from timing models can
  - Cost re-spin of the IP timing models at SoC level or in worst case at Silicon level.
  - Hurt **T**ime **T**o **M**arket (TTM) of the product.
  - Cost billions of dollars to the product revenue.

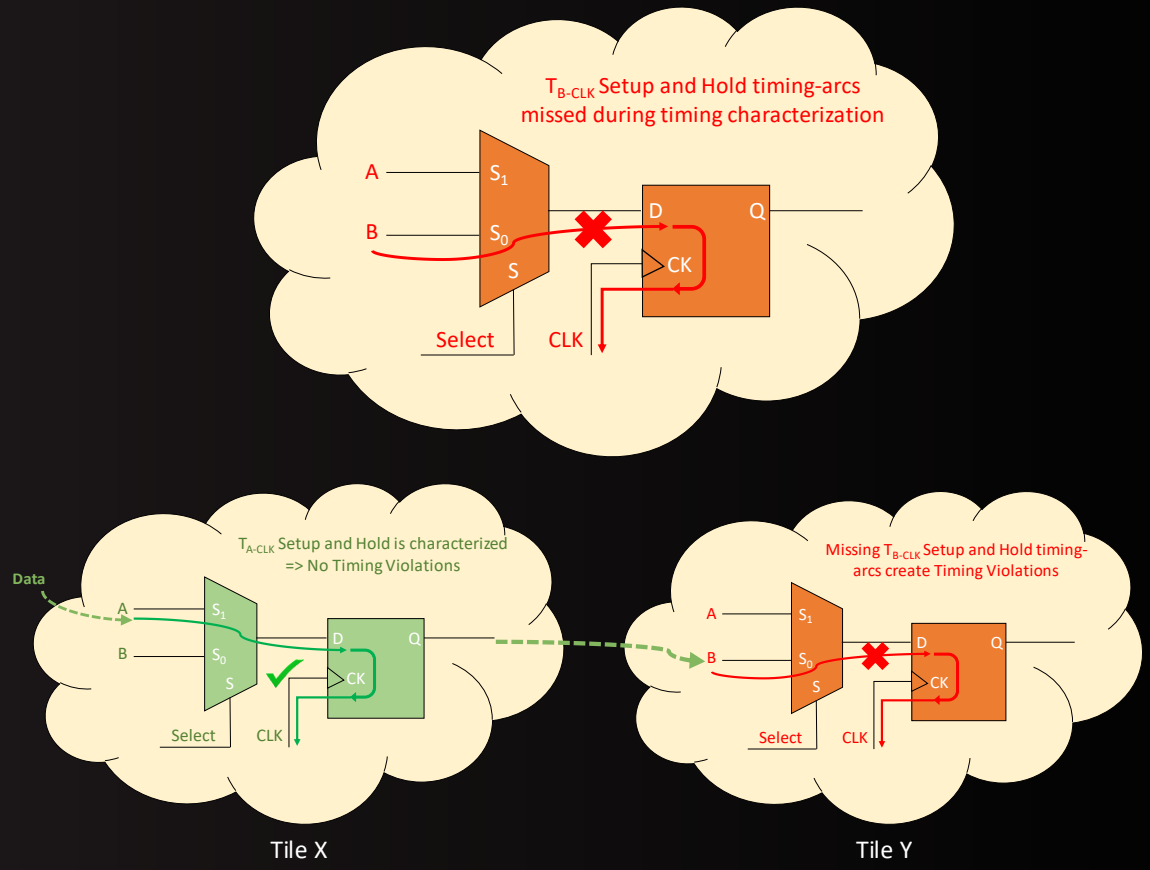


Fig. 1. Illustration of missed timing-arc situation during timing library characterization.

PROBLEM STATEMENT

- RTL
  - Most accurate modelling of the IP.
  - Goes through rigorous verification & validation at
    - IP level.
    - Integrated SoC level.
  - Can be used to identify timing-arcs.
- A well written “Design Constraint” file makes the timing models comprehensive.
  - Manual writing of this file may be prone to human error(s).
- Hence, there is a need to bridge the gap between these two.

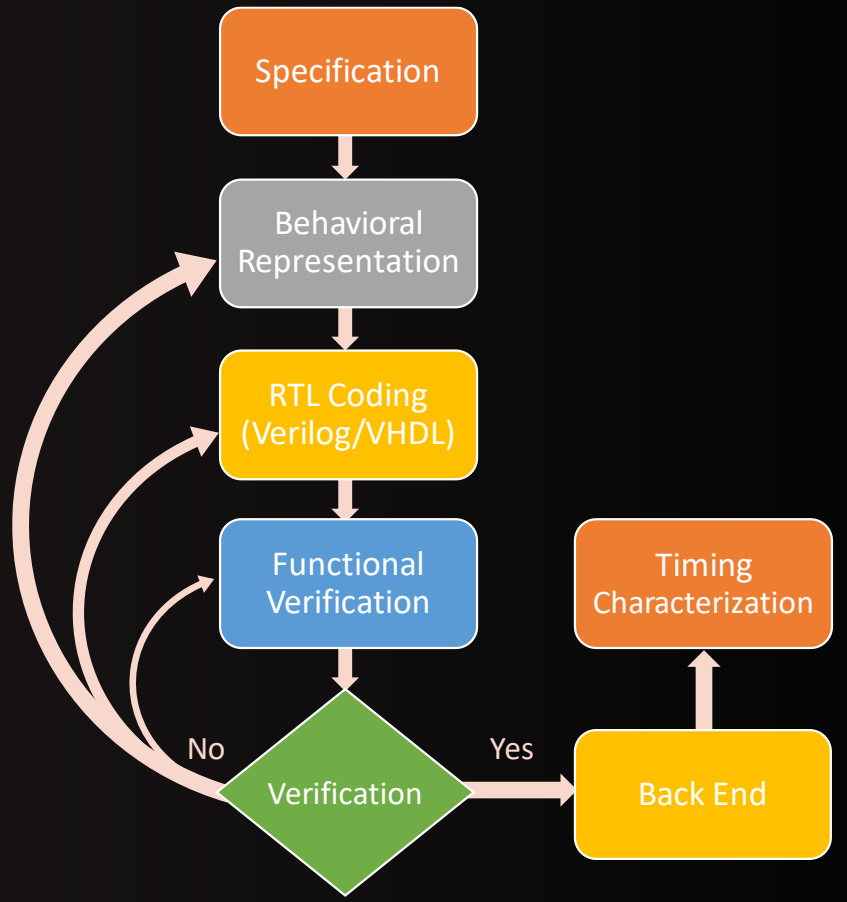


Fig. 2. ASIC VLSI Design Flow.

PROBLEM STATEMENT (CONTD.)

- Proposal: A software based RTL parser that generates timing-arcs based on different RTL constructs.
- Following timing-arcs can be inferred from the RTL description.

```
output [7:0] out;
input [7:0] data;
input load, enable, clk, reset;
reg [7:0] out;

always @(posedge clk)
if (reset) begin
  out <= 8'b0 ;
end else if (load) begin
  out <= data;
end else if (enable) begin
  out <= out + 1;
end
```

Code 1. A Sample Verilog RTL.

A. Setup/Hold:

1. Clk -> Reset
2. Clk -> Load
3. Clk -> Data
4. Clk -> Enable

B. Output:

1. Clk -> Out

C. Clock Pulse Width:

1. Clk -> Clk

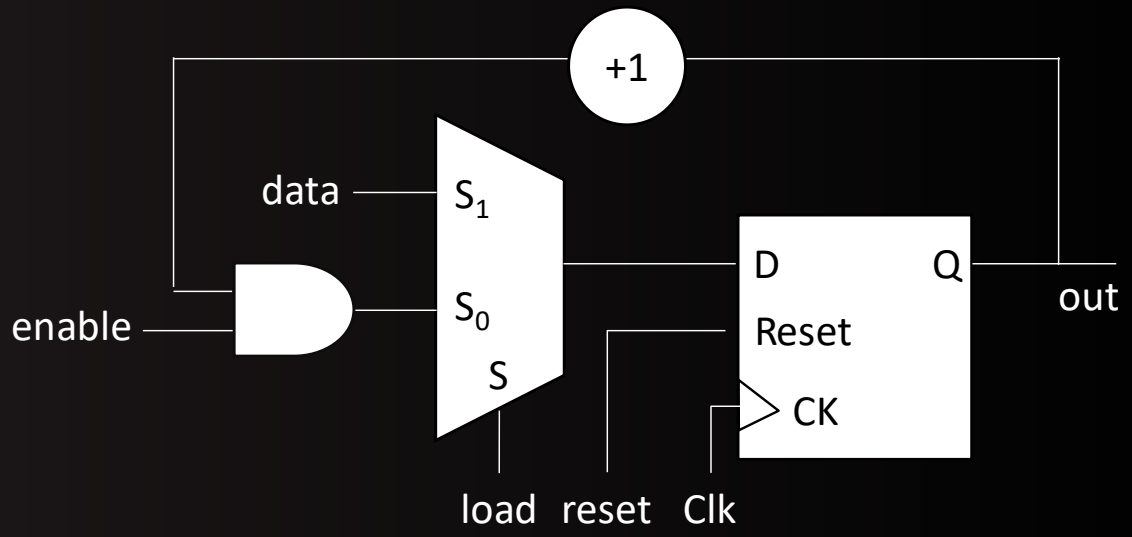


Fig. 3. Schematic of sample Verilog RTL.

SOLUTION

- RTLarc: An RTL based timing-arc tool
  - Reports timing-arc type and related pins after analyzing RTL.
  - Aids in comparison and verification of IP timing models.

Arc Number	Timing Arc		Timing-arc Type
	From	To	
1	Clk	Reset	Setup/Hold
2	Clk	Load	Setup/Hold
3	Clk	Data	Setup/Hold
4	Clk	Enable	Setup/Hold
4	Clk	Out	Output
5	Clk	Clk	Clock Pulse Width

Table 1. Sample output from RTLarc timing arc tool.

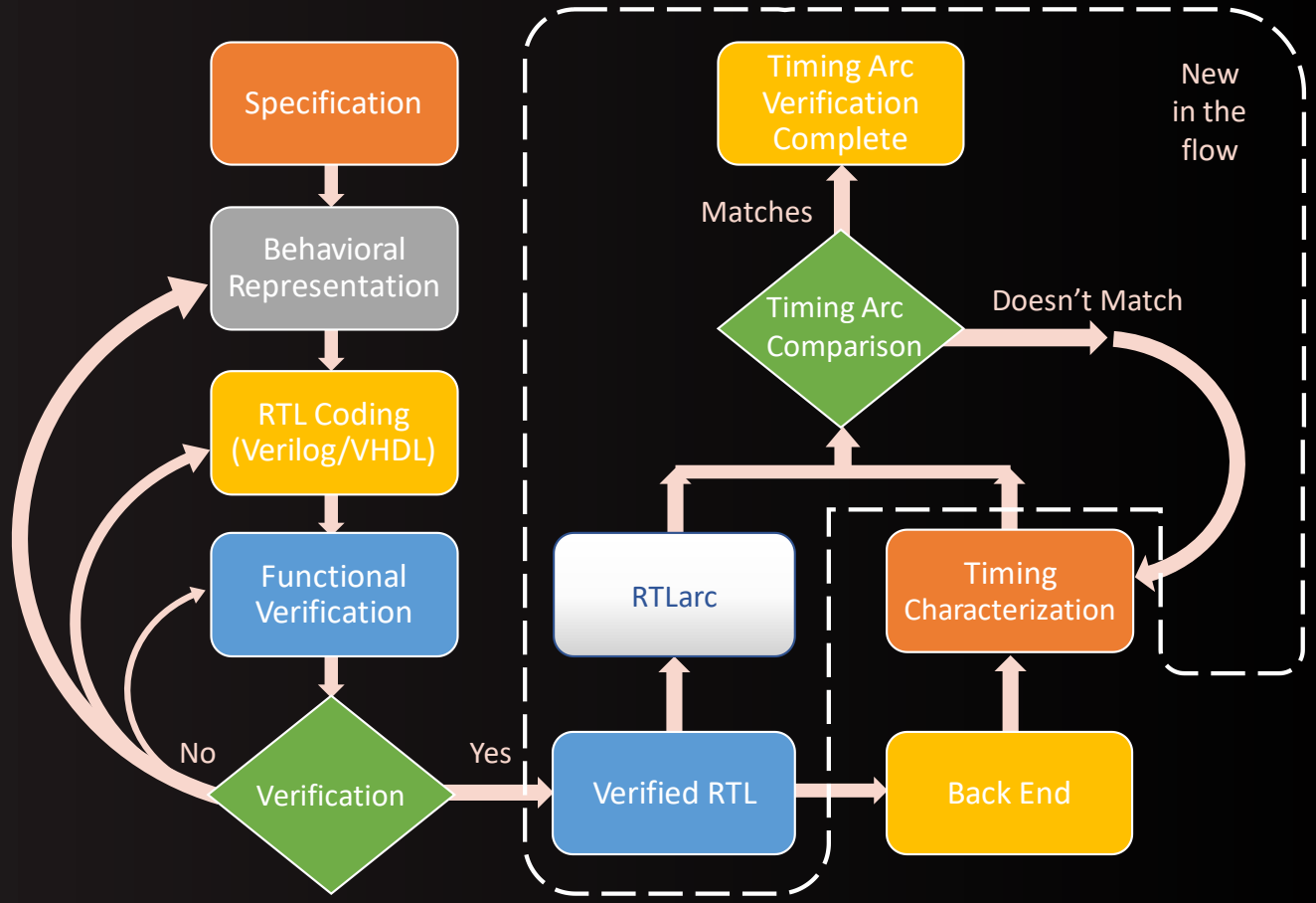
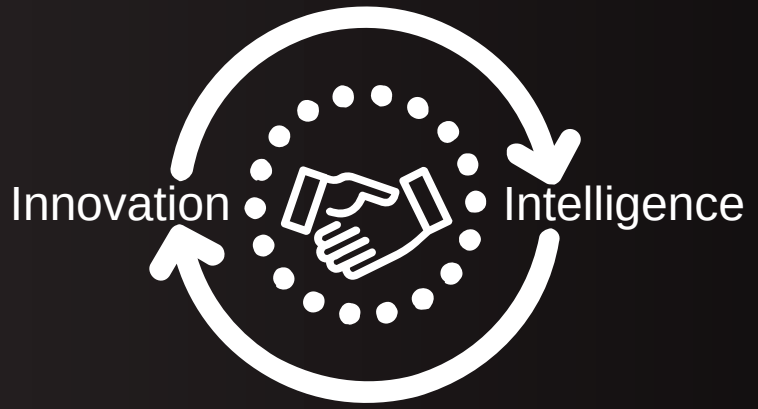


Fig. 4. ASIC VLSI Design Flow with RTLarc.

SUMMARY

- In ASIC VLSI design flow, timing model generation is a crucial and tape-out sensitive aspect.
- Missing arcs in IP timing models due to human error is unacceptable.
- Our proposal is to use the proven RTL infrastructure that aids in software verification of the generated timing models.
- We aim to enhance the confidence of the designer for design closure.



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